REMARKS

The Examiner's Action mailed on July 17, 2006 has been received and its contents carefully considered. Claims 1-23 remain pending. Applicant notes with appreciation that the Examiner has indicated that claims 5, 9, and 19 contain allowable subject matter and would be allowed if rewritten in independent form including all of the limitations of the base claim and any intervening claims. For at least the following reasons, it is submitted that this application is in condition for allowance in its present condition.

Claims 1-4, 6-8, 10-18, and 20-23 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over the Applicants' Admitted Prior Art (AAPA) in view of Cheok et al. (Cheok), U.S. Patent No. 6732280. The rejection is respectfully traversed.

Regarding claim 1, the Office Action points to the AAPA as allegedly teaching the invention essentially as claimed, including: (a) enabling the CPU to output a power management signal to the south bridge via the north bridge (*citing* page 2 lines 6-8); (b) enabling the south bridge to respond with a stop clock cycle to the CPU according to the power management signal (*citing* page 2 lines 10-11); (c) enabling the CPU to respond with a stop grant message according to the stop clock signal (*citing* page 2 lines 13-14); (d) enabling the north bridge to receive the stop grant message and at least one peripheral coupled to the north bridge (*citing* page 2 lines 15 and page 3 lines 1-4); (e) enabling the north bridge to pass the stop grant message to the south bridge after the north bridge receives the acknowledge signal (*citing* page 2 lines 15-16); (f) enabling the south bridge to output a power control signal after the south bridge receives the stop grant message (*citing* page 2 lines 17-18); and (g) enabling the power supply to

suspend a corresponding power after the power supply receives the power control signal (*citing* page 2 lines 22-23).

However, the Examiner acknowledges that the AAPA does not teach enabling the north bridge to analyze a power supply mode in the stop grant message, and enabling the north bridge to output a state transition signal to the at least one peripheral if the power supply mode is to suspend a main power supplied from the power supply or enabling the at least one peripheral to respond with an acknowledge signal after the at least one peripheral finishes its state transition according to the state transition signal. In short, the Examiner admits that the AAPA does not teach notifying peripherals coupled to a bridge to prepare for a transition to a sleep state if a transition for a system to enter a sleep state is required.

To address this shortcoming in the teaching of the AAPA, the Examiner points to Cheok allegedly as teaching a bridge notifying peripherals (via microcontroller 300) of an impending request to transition a system to a sleep state, the peripherals then perform "housekeeping" functions, and then send an acknowledgement in order to finish the transition (*citing* col. 4 line 27-37, col. 10 line 60 - col. 11 line 3 and col. 11 lines 27-30). The Office Action alleges that it would have been obvious to one of ordinary skill in the art at the time of the invention to include the teachings of Cheok into AAPA system, "because it would provide a means for peripheral devices to enter and exit sleep states in synchronism with a processor thus reducing the likelihood of failure for the devices on a subsequent boot operation (abstract and col. 2 lines 33-34)." (Office Action, p. 3) Applicants respectfully disagree with this position.

In contrast to the position taken by the Office Action, what the AAPA actually teaches is a prior computer system that includes a CPU, a north bridge communicating

with the CPU according to a hyper transport I/O link protocol, a south bridge, a power supply and at least one peripheral electrically connected to the north bridge. In power management operation, when the computer enters the power-saving mode, the CPU outputs a power management signal to the south bridge. The south bridge responds with a stop clock signal, and then the CPU responds with a stop grant message. The north bridge receives and analyzes the stop grant message to identify a power supply mode. If the power supply mode is to suspend the main power supplied from the power supply, the north bridge outputs a state transition signal to the peripheral. The north bridge receives an acknowledge signal from the peripheral and passes the stop grant message to the south bridge after receiving the acknowledge signal. The south bridge receives the stop grant message and outputs a power control signal accordingly. The power supply receives the power control signal for suspending the corresponding power accordingly.

The two short citations in Cheok, referenced by the Examiner, read as follows:

- "The PCI/ISA bridge (24) notifying peripherals (68, 70, 72, and 74) via microcontroller (300) of impending request to transition a system to a sleep state."
- "The peripherals (68, 70, 72, and 74) then perform "housekeeping" function then send an acknowledgement via microcontroller (300) to the PCI/ISA bridge (24) in order to finish the transition."

(col. 4 lines 27-43, col. 10 line 60 – col. 11 line 3 and col. 11 lines 27-30; *emphasis added*).

The above quoted language represents the sum and substance of the teaching of Cheok, with regard to peripherals coupling to the PCI/ISA bridge via the microcontroller to prepare for a transition to a sleep state. As can be readily verfied

from even a cursory reading of these segments, there is no suggestion at all in Cheok that any sort of north bridge in a computer system can be replaced by an ISA bridge. The north bridge is connected directly between the CPU and the system components, characterized with higher efficiency, high-speed link, and better performance, which are exemplified as cache, DRAM, peripherals of PCI express, and so on, as disclosed in the present application, rather than floppy disk drive (74), serial ports (72), mouse/trackball (70), and keyboard (68).

To the contrary, the PCI/ISA bridge does not connect to the CPU directly nor the peripherals of PCI express. The PCI/ISA bridge is connected to the CPU via a further host bridge, or a host bridge and a PCI bus. As disclosed in Cheok, the PCI/ISA bridge is connected to CPU (Pentium II processor module) 30 via a further host bridge 14 (col. 3 lines 49-51, FIG. 1). However, the north bridge of the present application connects the peripherals without any microcontroller. That is, compare to the embodiments of the present application, the PCI/ISA bridge of Cheok cannot be connected to the CPU directly. In addition, the PCI/ISA bridge cannot be connected to the peripherals of PCI express.

As will be appreciated by to those skilled in the art, the Examiner's proposed combination of Cheok with the AAPA would not result in the claimed embodiments.

The Examiner further asserts that hyper transport I/O link protocol is well known in the art to couple a processor with a north bridge. The Examiner, accordingly, asserts that it would be obvious that the processor in the AAPA would be coupled to the north bridge via hyper transport I/O link because it provides a high-speed link between the high-speed processor and north bridge. However, both a PCI/ISA bridge, a non-high speed link bridge, which is unable to be connected to CPU directly, and peripherals,

such as floppy disk drive (74), serial ports (72), mouse/trackball (70), and keyboard (68) of Cheok, are not compatible with the hyper transport I/O link protocol. For at least these reasons, the Examiner's proposed combination of Cheok with the AAPA would not result in the claimed invention.

Regarding claim 3, the Examiner points to Cheok as teaching preparing the devices for sleep (*see e.g.,* col. 10 line 60 – col. 11 line 3). This is interpreted as a L2/L3 ready state. Applicants respectfully disagree with this position. The L2/L3 ready state is for peripherals of PCI express. However, peripherals which are connected to PCI/ISA bridge via the PCI bus are not peripherals of PCI express. That is, the L2/L3 ready state of claim 3 is non-obvious to the AAPA and Cheok system.

Regarding claim 4, the Examiner alleges that the AAPA-Cheok system would comprise a decoder so that the power management signals sent from the processor could be recognized therefore enabling the system to act accordingly. Without a decoder, it would be impossible to distinguish the power management signals from other sent from either the processor or other device within the system. Applicants respectfully disagree with the Examiner's position. If the sleep state instruction transmitted from the CPU 30 via host bridge 14 to the PCI/ISA bridge can be directly recognized by the PCI/ISA bridge, the PCI/ISA bridge can transmit the sleep state instruction to peripherals via microcontroller without any decoder.

For at least the foregoing reasons, the rejections of independent claim 1, as well as dependent claims 2-5, should be withdrawn. Further, independent claims 6 and 10, which include defining limitations similar to those of claim 1 (as well as the claims 7-9 and claims 11-23 dependent therefrom respectively), patently define over the cited art as well.

As a separate and independent basis for the patentability of all claims, Applicant respectfully traverses the rejections as failing to identify a proper basis for combining the cited references. In combining these references, the Office Action stated only that the combination would have been obvious "because it would provide a means for peripheral devices to enter and exit sleep states in synchronism with a processor thus reducing the likelihood of failure for the devices on a subsequent boot operation." (Office Action, page 3). This alleged motivation is clearly improper in view of well-established Federal Circuit precedent.

It is well-settled law that in order to properly support an obviousness rejection under 35 U.S.C. § 103, there must have been some teaching in the prior art to suggest to one skilled in the art that the claimed invention would have been obvious. W. L. Gore & Associates, Inc. v. Garlock Thomas, Inc., 721 F.2d 1540, 1551 (Fed. Cir. 1983). More significantly,

> "The consistent criteria for determination of obviousness is whether the prior art would have suggested to one of ordinary skill in the art that this [invention] should be carried out and would have a reasonable likelihood of success, viewed in light of the prior art. ..." Both the suggestion and the expectation of success must be founded in the prior art, not in the applicant's disclosure... In determining whether such a suggestion can fairly be gleaned from the prior art, the full field of the invention must be considered; for the person of ordinary skill in the art is charged with knowledge of the entire body of technological literature, including that which might lead away from the claimed invention."

(*Emphasis added.*) In re Dow Chemical Company, 837 F.2d 469, 473 (Fed. Cir. 1988).

In this regard, Applicant notes that there must not only be a suggestion to combine the functional or operational aspects of the combined references, but that the Federal Circuit also requires the prior art to suggest both the combination of elements and the structure resulting from the combination. Stiftung v. Renishaw PLC, 945 Fed.2d

1173 (Fed. Cir. 1991). Therefore, in order to sustain an obviousness rejection based upon a combination of any two or more prior art references, the prior art must properly suggest the desirability of combining the particular elements to derive a power management system for a computer, as claimed by the Applicant.

When an obviousness determination is based on multiple prior art references, there must be a showing of some "teaching, suggestion, or reason" to combine the references. Gambro Lundia AB v. Baxter Healthcare Corp., 110 F.3d 1573, 1579, 42 USPQ2d 1378, 1383 (Fed. Cir. 1997) (also noting that the "absence of such a suggestion to combine is dispositive in an obviousness determination").

Evidence of a suggestion, teaching, or motivation to combine prior art references may flow, inter alia, from the references themselves, the knowledge of one of ordinary skill in the art, or from the nature of the problem to be solved. See In re Dembiczak, 175 F.3d 994, 1000, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). Although a reference need not expressly teach that the disclosure contained therein should be combined with another, the showing of combinability, in whatever form, must nevertheless be "clear and particular." Dembiczak, 175 F.3d at 999, 50 USPQ2d at 1617.

If there was no motivation or suggestion to combine selective teachings from multiple prior art references, one of ordinary skill in the art would not have viewed the present invention as obvious. See In re Dance, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998); Gambro Lundia AB, 110 F.3d at 1579, 42 USPQ2d at 1383 ("The absence of such a suggestion to combine is dispositive in an obviousness determination.").

Significantly, where there is no apparent disadvantage present in a particular prior art reference, then generally there can be no motivation to combine the teaching of

another reference with the particular prior art reference. Winner Int'l Royalty Corp. v. Wang, No 98-1553 (Fed. Cir. January 27, 2000). The rationales relied on by the Office Action in the present application are merely generic statements, that have nothing to do specifically with the structures disclosed in the other references. As such, these rationales cannot be properly viewed as proper motivations for combining the specific teachings of the individual references. Indeed, the generic motivations advanced by the present Office Action could be used to support a combination of ANY references, which is clearly contra to the cited Federal Circuit precedent and the clear intent of 35 U.S.C. § 103.

For at least the additional reason that the Office Action failed to identify proper motivations or suggestions for combining the various references to properly support the rejections under 35 U.S.C. § 103, those rejections should be withdrawn.

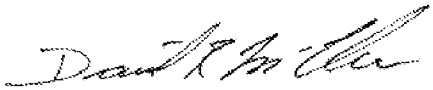
CONCLUSION

Based on the above, it is submitted that this application is in condition for allowance and such a Notice, with allowed claims 1-23, earnestly is solicited.

If the Examiner believes that a conference would be of value in expediting the prosecution of this application, the Examiner is hereby invited to telephone the undersigned counsel to arrange for such a conference.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

By: 

Daniel R. McClure
Registration No. 38,962

Thomas, Kayden, Horstemeyer & Risley, LLP
100 Galleria Pkwy, NW
Suite 1750
Atlanta, GA 30339
770-933-9500